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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/212,291	12/16/98	PRUDVI C	2207/5915

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EXAMINER	
WILLIAMS II,J	

ART UNIT	PAPER NUMBER
2751	

DATE MAILED: 08/18/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/212,291	PRUDVI ET AL.	
	Examiner	Art Unit	
	Jan S. Williams II	2751	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *16 December 1998* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected too by the draftsperson see attached copy of the PTO- 948.

Information Disclosure Statement

2. Applicant is reminded of the duty to disclose information concerning the pending application under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chittor et al. U.S. Patent NO. 6,061,764.

Chittor teaches as claimed:

A processing agent **(Chittor Figure 1 Ref No. 10)** adapted to transfer data of a predetermined data line in an external transaction **(Chittor Figure 1 Ref No. 60 shows a bus which is connected to the processing agent thus making it adapted to transfer data in an external transaction)**, the agent comprising an internal cache having a plurality of cache entries **(Chittor Figure 1 ref No. 14 shows the claimed internal cache)**, each entry adapted to store multiple data line lengths of data.

The processing agent of claim 1, wherein the cache entries include a cache coherency state field in association with each data line length of data. **(Chittor column 5 lines 38-49 teaches the claimed cache coherency state field which includes modified, read invalidate etc.)**

The agent of claim 1, further comprising a transaction queue having a plurality of queue entries **(Chittor Figure 2 ref No. 130 and ref No. 150 teach transaction queues)**, the queue entries including a primary entry adapted to store address information and status information of a first external transaction and a secondary entry adapted to store status information of a second external transaction **(Chittor column 4 lines 5-19 teaches that the queue as claimed holds information pertaining to the address of the transaction as well as status information)**.

The agent of claim 4, wherein the status information of the first external transaction included a field representing whether the first external transaction is part of a multiple transaction sequence. **(Chittor column 5 lines 1-9 teaches that a request is examined and from information which is part of the request (i.e. a field or**

section of bits within the request) the decoder can determine if the request is part of multiple transactions)

A processing agent **(Chittor Figure 1 ref No. 10)**, comprising a transaction queue having plurality of a queue entries **(Chittor figure 2 ref No. 130)**, the queue entries further comprising;

a primary entry including an address portion and status portion, the status portion provided for a first external transaction of the agent **(Chittor figure 2 ref No. 130 is shown with multiple entry spaces, also Chittor column 4 lines 5-19 teaches that the queue as claim holds information pertaining to the address of the transaction as well as status information)** and

a secondary entry including a status portion provided for second external transaction **(Chittor Figure 2 ref No. 130 as written above shows multiple entry lines which each indicate an entry into the queue).**

The transaction queue of claim 8, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction sequence. **(Chittor Figure 2 ref No. 130 shows the multiple entry lines within the queue, Chittor column 5 lines 1-9 teaches that a request is examined and from information which is part of the request (i.e. a field or section of bits within the request) the decoder can determine if the request is part of multiple transactions if the request is stored in the queue and the information which tells whether the transaction is part of multiple transaction is part of the request then that data is also stored in an entry within the queue)**

The transaction queue of claim 8, further comprising control logic adapted to cycle through the queue entries and post transaction therefrom. **(Chittor figure 2 ref No. 110 shows the decode circuit which performs the function of the control logic adapted to cycle through the queue entries.)**

A processing agent **(Chittor Figure 1 ref No. 10)**, comprising;

an internal cache having entries each adapted to store multiple data lines, and a transaction related to a single data line **(Chittor figure 1 ref No. 14)**,

wherein the internal cache and the transaction queue system each receive data requests on common input **(Chittor figure 1 ref No. 60 is a common input which is connected to the cache as well as the queue transaction)**.

The processing agent of claim 11, wherein the internal cache and the transaction queue system communicate by signal lines **(Chittor figure 1 ref No. 10 shows a signal line from the processor and cache going to the common bus and Chittor figure 2 shows a line coming form the transaction queue system to the common bus.)**

The processing agent of claim 11, wherein the transaction queue system comprises a plurality of queue entries, each queue entry comprising:

a primary entry including an address portion and status portion, the status portion provided for a first external transaction of the agent **(Chittor figure 2 ref No. 130 shows the entry within the queue, column 4 lines 5-19 teaches that the queue as claimed holds information pertaining to the address of the transaction as well as status information concerning the transactions)** , and

a secondary entry including a status portion provided for a second external transaction **(Chittor figure 2 ref No. 130 shows the entries within the queue, column 4 lines 5-19 teaches that the queue as claimed holds information pertaining to the address of the transaction as well as status information concerning the transactions)** .

The transaction queue of claim 14, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction sequence **(Chittor column 5 lines 1-9 teaches that the request is examined and from information which is part of the request (i.e. a field or section of bits within the request) the decoder can determine if the request is part of multiple transactions)**

The transaction queue of claim 14, further comprising control logic adapted to cycle through the queue entries and post transaction therefrom **(Chittor figure 2 ref No. 110 shows the decode circuit which performs the function of the control logic adapted to cycle through the queue entries.)**.

Claims 17-21 are the method claims of the above apparatus claims.

Related Art

4. **Pawlowski** U.S. Patent No. 5,696,910 teaches a method and apparatus for tracking transactions in a pipelined bus.

Sarangshar et al. U.S. Patent No. 5,796,977 teaches a highly pipelined bus architecture

Sarangshar et al. U.S. Patent No. 5,903,738 teaches a method and apparatus for performing bus transactions in a computer system.

Sarangshar et al. U.S. Patent No. 5,682,516 teaches a computer system that maintains system wide cache coherency during deferred communication transactions

Wang et al. U.S. Patent No. 5,642,494 teaches a cache memory with reduced request blocking

Conclusion

5. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 305-9051, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jan S. Williams II whose telephone number is (703) 306-5680. The examiner can normally be reached on Monday-Friday from 7:30 AM to 4:00 PM.

The examiner's supervisor, Eddie Chan, can be reached at (703) 305-9712.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900 or Tech Center 2700 Customer Service Office at (703) 306-5631.

JSW
August 9, 2000

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER